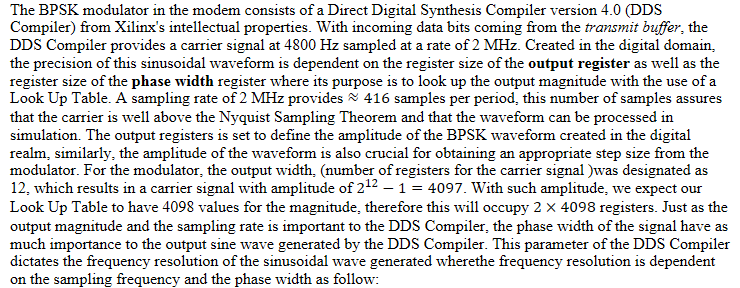
FEC-BPSK Modulator

Saturday, April 26, 2014

8:16 AM



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For modulating the phase of the carrier signal, a sub-module to the *Modulator.v* module is created named *mixer.v*. This sub-module sees as input the 4800 Hz carrier signal from the DDS Compiler and the data bits from the *receive buffer* and later modulates the phase of the signal based on the values of the bits. BPSK modulation is done by reversing the polarity of the BPSK signal with respect to the data bits a bit 0 consist of a 180◦, while a bit 1 is equal to a phase of 0◦. This can easily be implemented as an *if statement* (or some conditional statement similar to Simulink) with a rate of 1200 Hz to synchronize the phase changes to the sampling clock and the bit stream. However the latency present in the DDS Compiler and the sampling clock which is not a multiple of the carrier frequency slowly alters the phase value where the phase is set to change. Therefore, the phase changes were controlled to only change the phase when the phase is precisely equal to 0◦ or 180◦. Figure # illustrates the BPSK signal in the analog domain using the PmodDA2 Digital to Analog Converter (DAC) and the Fourier Transform obtained from the Electronics Explorer.

Figure #: BPSK signal generated using te0304 FPGA (a); FFT of BPSK signal obtained using Electronics Explorer (b)

